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UTILITY M PATENT APPLICATION TRANSMITTAL

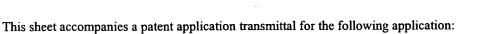
Title of Invention	Lateral Transistor Having Graded Base Region, Semiconductor Integrated Circuit And Fabrication Method Thereof				
Named Inventor(s)	Makoto Yamamoto; Akio Iwabuchi	164 194			
Attorney Docket	44471-265522 (13700)	25			
Express Mail Label No.	EL910717824US	00			

(Only for new nonprovisional applications under 37 CFR 1.53(b))

APPLICATION ELEMENTS		Assistant Commissioner for Patents ADDRESS TO: Box Patent Application Washington, D.C. 20231				
2. Applicat 2. Applicat 3. Specific and Abs 4. Drawing 5. Oath or Declar a. Newly e b. Copy fro	Total Sheets <u>9</u> Total Pages <u>32</u>	7. 8. 9.		c. Statement ver above copies Assignment: a. Assignment Paped document(s)) b. Assignment is or application No. 37 CFR 3.73(b) Statem (when there is an assignment is assignment is a assignment is a assignment is	no Acid Sequence le, all necessary) adable Copy dentical to computer copy) rifying identity of vers (cover sheet & f record in parent nent nent	
5b, is co accompa by refere (i)	nsidered as being part of the disclosure of the anying application and is hereby incorporated ence therein. DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b). the Computer Program (Appendix)	10. 11. 12. 13. 14.		Patent Application No. Other:	cument (if applicable) Statement (IDS) PTO- itations int rd (MPEP 503) itemized) ty Document(s) Japanese P2001-128187	
16. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information: Continuation Divisional Continuation-in-part (CIP) Of prior application No: Recite complete dependency back to first parent application: 17. CORRESPONDENCE ADDRESS						
☐ Customer Number or Bar Code Label 23370 (Insert Customer Atlantor Atlan						
Name (Print/Type) Telephone	Roger T. Frost (404)815-6500	Reg	gistrati	on No. (Attorney/Agent)	22,176	
Signature	MmT. France	Dat		26,2001	October 26, 2001	

FEE TRANSMITTAL





Makoto Yamamoto, et al. Inventor(s):

October 26, 2001 Filing Date:

Title:

Lateral Transistor Having Graded Base Region, Semiconductor

Integrated Circuit And Fabrication Method Thereof

The filing fee is calculated as shown below:

1. FILING FEE:

SMALL ENTITY

LARGE ENTITY

FOR:	FEE	FEE PAID	FEE	FEE PAID
UTILITY FILING FEE	\$370	\$	\$740	\$740
DESIGN FILING FEE	\$165		\$330	
PLANT FILING FEE	\$255		\$510	
REISSUE FILING FEE	\$370		\$740	
PROVISIONAL FILING FEE	\$80		\$160	
L Long to the state of the stat	SUBTOTAL (1)	\$		\$740

2. ECLAIMS:

SMALL ENTITY

LARGE ENTITY

FOR:	NO. FILED	NO. EXTRA	RATE	FEE	RATE	FEE
TOFAL CLAIMS	19 - 20 =	0	x 9 =	\$	x 18 =	\$0
INDEP. CLAIMS	3 - 3 =	0	x 42 =		x 84 =	0
"MULTIPLE DEPENDENT CLAIM PRESENTED +140 =		+140 =		+280 =		
		SUB	TOTAL (2)	\$		\$0

3. ADDITIONAL FEES:

	SMALI	LARGE ENTITY		
FOR:	FEE	FEE PAID	FEE	FEE PAID
LATE FILING, FEE OR OATH	\$65	\$	\$130	\$
NON-ENGLISH SPECIFICATION	\$130		\$130	
OTHER				
Name of the state	SUBTOTAL (3)	\$		\$

TOTAL FILING FEES: \$740

A check is enclosed for the total amount: \$740

Charge any additional fees required under 37 C.F.R. 1.16 or 1.17 to Deposit Account 11-0855.

John S. Pratt

KILPATRICK STOCKTON LLP

1100 Peachtree Street

Suite 2800

Atlanta, Georgia 30309-4530

Telephone: 404-815-6500

By: Roger T. Frost, Attorney for Applicant

Reg. No. 22,176

Date: October 26, 2001